IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/227,174	Confirmation No. 8615
Applicant	:	Thomas A. Piazza	
Filed	:	January 7, 1999	
TC/A.U.	:	2613	
Examiner	:	Richard J. Lee	
Docket No.	:	42390.P6702	
Customer No.	:	008791	

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant (hereafter "Appellant") hereby submits this Brief in triplicate in support of its appeal from a final decision by the Examiner, mailed May 27, 2003, in the above-referenced case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the present patent application.

An oral hearing is not desired.

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I. REAL PARTY IN INTEREST

The present U.S. Patent application is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal which will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF CLAIMS

Claims 29-50 are pending in the present application. Claims 1-28 have been canceled during prosecution. Claims 29-50 were rejected in the Final Office Action mailed May 27, 2003 and are the subject of this appeal.

Claim 33 stands rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 29, 31, 32, 41, 42, 45, and 48 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,652,823 issued to Eto (*Eto*) in view of U.S. Patent No. 5,337,086 issued to Fujinami (*Fujinami*) and further in view of U.S. Patent No. 6,002,438 issued to Hocevar, et al. (*Hocevar*). Claims 33, 34, 43, 44, 46, 47, 49, and 50 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Eto*, *Fujinami*, *Hocevar*, and further in view of U.S. Patent No. 5,892,518 issued to Mizobata, et al. (*Mizobata*). Claims 30 and 36-39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Eto*, *Fujinami*, *Hocevar*, and further in view of U.S. Patent No. 6,208,350 B1 issued to Herrera (*Herrera*). Claim 35 stands rejected under 35 U.S.C.

103(a) as being unpatentable over *Eto*, *Fujinami*, *Hocevar*, and further in view of U.S. Patent No. 5,446,495 issued to Tortier, et al. (*Tortier*). Claim 40 stands rejected under 35 U.S.C. 103(a) as being unpatentable over *Eto*, *Fujinami*, *Hocevar*, and *Herrera*, and further in view of *Tourtier*.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed May 27, 2003, rejecting claims 29-50, Applicant timely filed a Notice of Appeal on August 27, 2003.

A copy of all claims on appeal is attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

The present invention provides motion compensation decoding scheme wherein motion compensation of graphics with a texture mapping engine is performed. In general, the invention provides motion compensation by reconstructing a picture by predicting pixel colors from one or more reference pictures. See Specification at page 5, lines 1-2 and 13-14.

In one embodiment, a command stream controller receives commands from an external source and decodes the commands to perform appropriate control functions. See Specification at page 10, lines 18-20. Control information is sent to a write address generator while correction data is forwarded to and stored in a texture palette or other memory. The write address generator causes the correction data for pixels of a macroblock to be written into the texture palette in an order as output by an Inverse Discrete Cosine Transform (IDCT) operation for the macroblock. In one embodiment, the write address generator causes correction data for the pixels of a macroblock to be

written to the texture palette block by block in row major order. See Specification at page 11, lines 3-11 and 17-21.

In one embodiment, a fetch unit converts read addresses into cache addresses and the pixel data stored at the cache address is sent to a bilinear filter. See Specification at page 15, lines 5-7. The bilinear filter then sends pixel location information to a read address generator. The read address generator causes the correction data to be read from the texture palette in an order different from which it was written as controlled by the write address generator. In one embodiment, the read address generator causes correction data to be read from the texture palette sub-block by sub-block in row major order. See Specification at page 15, line 17 through page 16 line 3.

In one embodiment, frame prediction operations are performed for motion compensation. A windower iterates pixels within a bounding box and adds correction data to generate write addresses. See Specification at page 14, lines 13-14, and page 9 lines 13-16. A blend unit combines the pixel data from the bilinear filter with the correction data from the texture palette to generate an output pixel for a new video frame. See Specification at page 16, lines 10-12. A FIFO buffer is provided to allow memory latency to be hidden with respect to reference pixels, thereby improving pipeline performance. See Specification at page 16, lines 18-23.

VI. ISSUES PRESENTED

1. Whether claims 29, 31, 32, 41, 42, 45, and 48 are unpatentable under 35 U.S.C. 103(a) in view of *Eto* and *Fujinami*, and further in view of *Hocevar*.

2. Whether claims 33, 34, 43, 44, 46, 47, 49, and 50 are unpatentable under 35 U.S.C. 103(a) in view of *Eto*, *Fujinami*, and *Hocevar*, and further in view of *Mizobata*.

3. Whether claims 30 and 36-39 are unpatentable under 35 U.S.C. 103(a) in view of *Eto*, *Fujinami*, and *Hocevar*, and further in view *Herrera*.

4. Whether claim 35 is unpatentable under 35 U.S.C. 103(a) in view of *Eto*, *Fujinami*, and *Hocevar*, and further in view *Tortier*.

5. Whether claim 40 is unpatentable under 35 U.S.C. 103(a) in view of *Eto*, *Fujinami*, *Hocevar*, and *Herrera*, and further in view *Tortier*.

VII. GROUPING OF CLAIMS

The claims do not stand or fall together. For purposes of this appeal:

claims 29, 31, 32, 41, 42, 45, and 48 stand or fall together as Claim Group I;

claims 33, 34, 43, 44, 46, 47, 49, and 50 stand or fall together as Claim Group II;

claims 30 and 36-39 stand or fall together as Claim Group III;

claim 35 stands or falls as Claim Group IV;

claim 40 stands or falls as Claim Group V.

Reasons for separate patentability of the above-indicated Claim Groups I-V are presented in the arguments section pursuant to 37 C.F.R. § 1.192(c)(7).

VIII. ARGUMENTS

A. REJECTION OF CLAIMS 29, 31, 32, 41, 42, 45, AND 48 AS BEING UNPATENTABLE UNDER 35 U.S.C. 103(a) OVER *ETO* IN VIEW OF *FUJINAMI* AND FURTHER IN VIEW OF *HOCEVAR* IS IMPROPER BECAUSE *ETO*, *FUJINAMI*, AND *HOCEVAR* DO NOT CONTAIN ANY SUGGESTION (EXPRESS OR IMPLIED) THAT THEY BE COMBINED IN THE MANNER SUGGESTED.

In the Final Office Action mailed May 27, 2003, claims 29, 31, 32, 41, 42, 45, and 48 (Claim Group I) were rejected under 35 U.S.C. 103(a) as being unpatentable over *Eto* in view of *Fujinami* and further in view of *Hocevar*. Appellant respectfully submits that

claims 29, 31, 32, 41, 42, 45, and 48 are not obvious in view of *Eto*, *Fujinami*, and *Hocevar* for at least the reasons set forth below.

Appellant's claim 29 recites the following:

> a memory coupled to the command stream controller and to the write address generator, **the memory to store pixel data in a first order** determined by the write address generator;
> processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and
> a read address generator coupled to the processing circuitry and to the memory, **the read address generator to cause the memory to output pixel data in a second order**, wherein the second order comprises a sub-block by sub-block in row major order.

Thus, Appellant claims storing pixel data in a first order and outputting the pixel data in a second order. The write address generator causes pixel data of a macroblock to be written to memory block by block in row major order. The read address generator causes the pixel data to be read from the memory sub-block by sub-block in row major order - which order is different from the order in which it was written as controlled by the write address generator. Claims 41 and 45 are method claims that similarly recite storing pixel data in a first order and outputting the pixel data in a second order. Claim 48 is an article of manufacture claim that also recites similar limitations.

The Final Office Action mailed May 27, 2003, states that "*Eto* et al does not particularly disclose...(a) wherein the second order comprises reading the pixel data sub-block-by-sub-block [sic] row major order." *Fujinami* is then cited as teaching the "conventional breakdown of macroblocks into subblocks" at column 4, lines 39-52, columns 7-9, and figures 1 and 6. The Final Office Action then states that "*Fujinami* is silent as to whether the blocks and subblocks stored and retrieve [sic] from memory are

based on the row major orders as claimed." Finally, *Hocevar* is cited as teaching storage and retrieval of blocks in a row major order fashion at column 7, lines 9-48.

More succinctly, *Eto* is cited as disclosing storing data block by block, constituting a first order, and the combination of *Fujinami* and *Hocevar* are cited as disclosing the retrieval of data sub-block by sub-block in row major order, constituting a second order. Whether or not these references teach the above-cited limitations, they do not provide any suggestion or motivation that the references be combined. In other words, the simple assertion that *Eto* discloses reading and writing data in one order and that a combination of *Fujinami* and *Hocevar* discloses reading and writing data in another order does not reflect the complexity of reading data out in a different order from which it was originally written. The value of separate and individual components in this case is outweighed by the synergy of combining those components into a single and unified structure.

Having cited *Eto*, *Fujinami*, and *Hocevar* in the rejection of claims 29, 31, 32, 41, 42, 45, and 48 the Final Office Action, without further explanation, concludes:

> It is hence obvious to provide the row major order storage and retrieval of blocks as taught by Hocevar et al as the specific method for the processing of data within the memory system of Fujinami. Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto et al, Fujinami, and Hocevar et al references in front of him/her and the general knowledge of block processing within motion compensation video systems, would have had no difficulty in providing a first order..., storing the correction data in a memory block by block in row major order, and reading the pixel data in subblock by subblock major order...within Eto et al in view of the teachings of the combination of Fujinami and Hocevar et al for the same well known selective block processings as claimed.

The Final Office Action provides no evidence to support this conclusory statement. To support an explicit or implicit motivation, suggestion, or teaching to combine references,

particular findings of fact must be provided. *In re Kotzab*, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). Identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *Id* at 1316. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making **the specific combination** that was made by the applicant. *Id.*

Appellant further submits that the references fail to disclose "a write address generator" and "a read address generator" as recited by Appellant in claim 29. *Eto* is cited as disclosing these limitations at column 35, lines 13-30. *Eto* discusses a write/read control signal that triggers the temporal storage into memory of the output from a motion decoder. However, *Eto* fails to disclose a write address generator that determines the order in which pixel data will be written to memory and a read address generator that determines the order in which the data will be read out from memory as claimed by Appellant. Because *Eto* fails to disclose these limitations, the combination of *Eto*, *Fujinami*, and *Hocever* fails to disclose the invention as recited by Appellant in claim 29 regardless of a motivation to combine the references.

Claims 31 and 32 depend from claim 29. Claim 42 depends from claim 41. Claim 48 depends from claim 45. Given that dependent claims necessarily include the limitations of the claims from which they depend, Appellant submits that claims 31, 32, 42, and 48 are not obvious in view of *Eto* and *Fujinami*, and further in view of *Hocevar* for at least the reasons set forth above with respect to claims 29, 41, and 45.

For at least the foregoing reasons Appellant submits that there is no motivation to combine *Eto*, *Fujinami* and *Hocevar* to achieve the invention as claimed in claims 29, 31,

32, 41, 42, 45, and 48. Appellant therefore requests that the Board of Patent Appeals and Interferences overrule the Examiner's rejection of claims 29, 31, 32, 41, 42, 45, and 48 under 35 U.S.C. 103(a).

B. REJECTION OF CLAIMS 33, 34, 43, 46, 47, 49, AND 50 AS BEING UNPATENTABLE UNDER 35 U.S.C. 103(a) OVER THE COMBINATION OF *ETO*, *FUJINAMI*, AND *HOCEVAR*, AND FURTHER IN VIEW OF *MIZOBATA* IS IMPROPER BECAUSE *ETO*, *FUJINAMI*, *HOCEVAR* AND *MIZOBATA* DO NOT CONTAIN ANY SUGGESTION (EXPRESS OR IMPLIED) THAT THEY BE COMBINED IN THE MANNER SUGGESTED.

In the Final Office Action mailed May 27, 2003, claims 33, 34, 43, 44, 46, 47, 49, and 50 (Claim Group II) were rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of *Eto*, *Fujinami*, and *Hocevar* and further in view of *Mizobata*. Appellant respectfully submits that claims 33, 34, 43, 44, 46, 47, 49, and 50 are not obvious in view of *Eto*, *Fujinami*, *Hocevar*, and *Mizobata*.

Claims 33 and 34 depend from claim 29. Claims 43 and 44 depend from claim 41. Claims 46 and 47 depend from claim 45. Claims 49 and 50 depend from claim 48. Claims 29, 41, 45, and 48 are part of Claim Group I, which is discussed above. Therefore, the arguments above with respect to Claim Group I are incorporated by reference with respect to Claim Group II.

The claims of Claim Group II are directed to a bounding box and processing of pixels within the bounding box. The Final Office Action states that *Mizobata* discloses the following:

> ...substantially the same frame prediction operations comprising means for generating a bounding box, means for iterating the bounding box, means for fetching reference pixels, means for filtering the reference pixels, means for averaging the filtered reference pixels, if necessary, and

means for adding correction data to the reference pixels; means for performing texturing operations for the macroblock; and processing circuitry comprising a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock and wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the bounding box are processed.

Whether or not *Mizobata* discloses the limitations cited by the Final Office Action, it does not teach or suggest storing pixel data in a first order and outputting pixel data in a second order as claimed by Appellant. Therefore, *Mizobata* fails to cure the deficiencies of *Eto*, *Fujinami*, and *Hocevar* discussed above with respect to Claim Group I. Thus, Appellant respectfully submits that no combination of *Eto*, *Fujinami*, *Hocevar*, and *Mizobata* renders claims 33, 34, 43, 46, 47, 49, and 50 obvious.

For at least the foregoing reasons Appellant submits that there is no motivation to combine *Eto*, *Fujinami*, *Hocevar*, and *Mizobata* to achieve the invention as claimed in claims 33, 34, 43, 46, 47, 49, and 50. Appellant therefore requests that the Board of Patent Appeals and Interferences overrule the Examiner's rejection of claims 33, 34, 43, 46, 47, 49, and 50 under 35 U.S.C. 103(a).

C. REJECTION OF CLAIMS 30 AND 36-39 AS BEING UNPATENTABLE UNDER 35 U.S.C. 103(a) OVER THE COMBINATION OF *ETO*, *FUJINAMI*, AND *HOCEVAR*, AND FURTHER IN VIEW OF *HERRERA* IS IMPROPER BECAUSE *ETO*, *FUJINAMI*, *HOCEVAR* AND *HERRERA* DO NOT CONTAIN ANY SUGGESTION (EXPRESS OR IMPLIED) THAT THEY BE COMBINED IN THE MANNER SUGGESTED.

In the Final Office Action mailed May 27, 2003, claims 30 and 36-39 (Claim Group III) were rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of *Eto*, *Fujinami*, and *Hocevar* and further in view of *Herrera*. Appellant

respectfully submits that claims 30 and 36-39 are not obvious in view of *Eto*, *Fujinami*, *Hocevar*, and *Herrera*.

Claim 30 depends from claim 29. Claim 29 is part of Claim Group I, which is discussed above. Therefore, the arguments above with respect to Claim Group I are incorporated by reference with respect to Claim Group III.

Claim 36 recites the following:

> a command stream controller to manipulate motion compensation video data;
>
> a memory coupled to the command stream controller, the memory **to store pixel data related to a macroblock in a first order**, the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation; and
>
> a read address generator coupled to the memory, the read address generator to cause the memory **to output the pixel data related to a macroblock in a second order**, the read address generator to cause the memory to output pixel data in sub-block-by-sub-block in row major order; and
>
> a processing unit coupled to the read address generator and to the command stream controller, the processing unit to perform motion compensation operations and texture mapping operations utilizing common circuitry.

Thus, Appellant claims storing pixel data related to a macroblock in a first order and outputting the pixel data related to a macroblock in a second order. The write address generator causes pixel data of a macroblock to be written block by block in row major order. The read address generator causes the pixel data to be read in an order different from which it was written as controlled by the write address generator. The processing unit performs texture mapping operations utilizing common circuitry. Claims 37-39 depend from claim 36.

The Final Office Action states that *Herrera* discloses "the conventional texture mapping operations and bilinear filterings with motion compensation systems." Whether

or not *Herrera* discloses the limitations cited by the Final Office Action, it does not teach or suggest storing pixel data in a first order and outputting pixel data in a second order as claimed by Appellant. Therefore, *Herrera* fails to cure the deficiencies of *Eto*, *Fujinami*, and *Hocevar* discussed above with respect to Claim Group I. Thus, Appellant respectfully submits that no combination of *Eto*, *Fujinami*, and *Hocevar*, and *Herrera* renders claims 30 and 36-39 obvious.

Appellant further submits that there is no suggestion or motivation to combine *Herrera* with *Eto*. *Eto* discloses an apparatus that performs video encoding and video decoding. See, e.g., FIG. 1 and FIG. 7. *Herrera*, in contrast, discloses a combination of a modified graphics accelerator with software to create a cost effective hybrid solution to providing a personal computer with DVD capabilities. See, e.g., column 4, lines 63-66 and FIG. 8. *Herrera* states:

> The second type of solution, places the DVD processing task entirely on the PC's hardware ... providing such specialized circuitry (**e.g., a DVD decoder**) can be very expensive and result in significantly increased costs, which can be **devastating** in the highly competitive PC market. The specialized circuitry can also **reduce the performance of the PC** by requiring access to the PC's bus(es), interfaces and memory components, in some PC architectures.

See column 4, lines 37-46. *Herrera*, therefore, explicitly **teaches away** from *Eto*, rather than providing an implicit basis to combine the references. Because *Herrera* explicitly teaches away from *Eto*, Appellant respectfully submits that the combination of *Herrera* with *Eto* is improper.

For at least the foregoing reasons, Appellant submits that there is no motivation to combine *Eto*, *Fujinami*, *Hocevar*, and *Herrera* to achieve the invention as claimed in claims 30 and 36-39. Appellant therefore requests that the Board of Patent Appeals and

Interferences overrule the Examiner's rejection of claims 30 and 36-39 under 35 U.S.C. 103(a).

D. REJECTION OF CLAIM 35 AS BEING UNPATENTABLE UNDER 35 U.S.C. 103(a) OVER THE COMBINATION OF *ETO*, *FUJINAMI*, AND *HOCEVAR* AND FURTHER IN VIEW OF *TOURTIER* IS IMPROPER BECAUSE *ETO*, *FUJINAMI*, *HOCEVAR* AND *TOURTIER* DO NOT CONTAIN ANY SUGGESTION (EXPRESS OR IMPLIED) THAT THEY BE COMBINED IN THE MANNER SUGGESTED.

In the Final Office Action mailed May 27, 2003, claim 35 (Claim Group IV) was rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of *Eto*, *Fujinami*, and *Hocevar* and further in view of *Tourtier*. Appellant respectfully submits that claim 35 is not obvious in view of *Eto*, *Fujinami*, *Hocevar*, and *Tourtier*.

Claim 35 depends from claim 29. Claim 29 is part of Claim Group I, which is discussed above. Therefore, the arguments above with respect to Claim Group I are incorporated by reference with respect to Claim Group IV.

The Final Office Action states that "the particular motion compensation pipeline processings are old and well recognized in the art, as exemplified by *Tourtier*." Whether or not *Tourtier* discloses the limitations cited by the Final Office Action, it does not teach or suggest storing pixel data in a first order and outputting pixel data in a second order as claimed by Appellant. Therefore, *Tourtier* fails to cure the deficiencies of *Eto*, *Fujinami*, and *Hocevar* discussed above with respect to Claim Group I.

Furthermore, the simple reference to *Tourtier*, declaring that pipelining is well-known generally, does not relieve the burden of demonstrating obviousness by a showing of particular findings of fact. *In re Kotzab* (2000). In other words, citing *Tourtier* does not, in and of itself, address the complexities of storing data in a first order and reading

out data in a second order within the framework of pipelined circuitry. Appellant submits that *Tourtier* does not teach, suggest, or address these complexities. Thus, Appellant respectfully submits that no combination of *Eto*, *Fujinami*, *Hocevar*, and *Tourtier* renders claim 35 obvious.

For at least the foregoing reasons Appellant submits that there is no motivation to combine *Eto*, *Fujinami*, *Hocevar*, and *Tourtier* to achieve the invention as claimed in claim 35. Appellant therefore requests that the Board of Patent Appeals and Interferences overrule the Examiner's rejection of claim 35 under 35 U.S.C. 103(a).

E. REJECTION OF CLAIM 40 AS BEING UNPATENTABLE UNDER 35 U.S.C. 103(a) OVER THE COMBINATION OF *ETO*, *FUJINAMI*, *HOCEVAR*, AND *HERRERA*, AND FURTHER IN VIEW OF *TOURTIER* IS IMPROPER BECAUSE *ETO*, *FUJINAMI*, *HOCEVAR*, *HERRERA* AND *TOURTIER* DO NOT CONTAIN ANY SUGGESTION (EXPRESS OR IMPLIED) THAT THEY BE COMBINED IN THE MANNER SUGGESTED.

In the Final Office Action mailed May 27, 2003, claim 40 (Claim Group V) was rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of *Eto*, *Fujinami*, *Hocevar*, and *Herrera*, and further in view of *Tourtier*. Appellant respectfully submits that claim 40 is not obvious in view of *Eto*, *Fujinami*, *Hocevar*, *Herrera* and *Tourtier*.

Claim 40 depends from claim 36. Claim 36 is part of Claim Group III, which is discussed above. Claim Group III incorporates by reference the arguments of Claim Group I. Therefore, the arguments above with respect to Claim Groups I and III are incorporated by reference with respect to Claim Group V.

The Final Office Action states that "the particular motion compensation pipeline processings are old and well recognized in the art, as exemplified by *Tourtier*." Whether or not *Tourtier* discloses the limitations cited by the Final Office Action, it does not teach or suggest storing pixel data in a first order and outputting pixel data in a second order as claimed by Appellant. Therefore, *Tourtier* fails to cure the deficiencies of *Eto*, *Fujinami*, and *Hocevar* discussed above with respect to Claim Group I. Appellant further points out the arguments made with respect to Claim Group IV showing that there is no motivation to combine *Eto* and *Herrera*. Thus, Appellant submits that no combination of *Eto*, *Fujinami*, *Hocevar*, *Herrera*, and *Tourtier* renders claim 40 obvious.

For at least the foregoing reasons Appellant submits that there is no motivation to combine *Eto*, *Fujinami*, *Hocevar*, *Herrera*, and *Tourtier* to achieve the invention as claimed in claim 40. Appellant therefore requests that the Board of Patent Appeals and Interferences overrule the Examiner's rejection of claim 40 under 35 U.S.C. 103(a).

IX. CONCLUSION

Appellant respectfully submits that all the appealed claims in this application are patentable and requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $330.00 to cover the appeal fee for one other than small entity as specified in 37 C.F.R. 6 1.17(f). Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Date: Nov 21, 2003

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X. APPENDIX OF CLAIMS

29. A circuit for generating motion compensated video, the circuit comprising:

a command stream controller to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output pixel data in a second order, wherein the second order comprises a sub-block-by-sub-block in row major order.

30. The circuit of claim 29, wherein the processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame comprises processing circuitry to perform motion compensation operations and texture mapping operations utilizing common circuitry.

31. The circuit of claim 29, wherein the first order corresponds to an output sequence of an inverse discrete cosine transform operation.

32. The circuit of claim 29, wherein the first order is block by block in row major order.

33. The circuit of claim 29,

wherein a command stream controller to manipulate motion compensated video data comprises a command stream controller coupled to receive an instruction to manipulate motion compensated video; and

wherein the processing circuitry comprises a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock.

34. The circuit of claim 29, wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed, and a second mode wherein all pixels within the bounding box are processed.

35. The circuit of claim 29, wherein the circuit is pipelined.

36. An apparatus comprising:

a command stream controller to manipulate motion compensation video data;

a memory coupled to the command stream controller, the memory to store pixel data related to a macroblock in a first order, the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation;

a read address generator coupled to the memory, the read address generator to cause the memory to output the pixel data related to a macroblock in a second order, the read address generator to cause the memory to output pixel data in sub-block-by-sub-block in row major order; and

a processing unit coupled to the read address generator and to the command stream controller, the processing unit to perform motion compensation operations and texture mapping operations utilizing common circuitry.

37. The apparatus of claim 36, wherein the memory to store pixel data related to a macroblock in a first order comprises the memory to store pixel data related to a macroblock block by block in row major order.

38. The apparatus of claim 36, wherein the processing unit further comprises:

a memory to store reference pixels;

a mapping address generator to provide read addresses for the reference pixels;

a bilinear filter coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels; and

a first-in-first-out (FIFO) buffer coupling the mapping address generator to the bilinear filter, the buffer to maintain sequence of the read addresses from the mapping address generator to the bilinear filter.

39. The apparatus of claim 36, further comprising the read address generator coupled to a write address generator, the write address generator to generate synch points and the

read address generator to receive the synch points to prevent the read address generator from overwriting valid data in the memory.

40. The apparatus of claim 36, wherein the apparatus is pipelined.

41. A method comprising:

storing pixel data in a memory in a first order based on output from an Inverse Discrete Cosine Transform (IDCT) operation;

receiving a command to generate a reconstructed video frame; and

reading the pixel data out of the memory in a second order, wherein the second order comprises reading the pixel data sub-block-by-sub-block in row major order.

42. The method of claim 41, wherein storing pixel data in a memory in a first order based on output from an Inverse Discrete Cosine Transform (IDCT) operation comprises storing pixel data block by block in row major order.

43. The method of claim 41, further comprising determining a bounding box for pixels manipulated by the command, wherein the bounding box contains all edges of a macroblock.

44. The method of claim 43, further comprising processing the pixel data in triangular regions, wherein in a first mode pixels inside a triangle within a bounding box are processed, and in a second mode all pixels within the bounding box are processed.

45. A method of motion compensation of digital video data, the method comprising:

receiving a motion compensation command having associated correction data related to a macroblock;

storing the correction data in a memory block by block in row major order;

performing frame prediction operations in response to the motion compensation command;

reading the correction data from the memory sub-block by sub-block in row major order; and

combining the correction data with results from the frame prediction operations to generate an output video frame.

46. The method of claim 45, wherein performing frame prediction operations further comprises:

generating a bounding box containing the macroblock; and

iterating the bounding box;

fetching reference pixels;

filtering the reference pixels;

averaging the filtered reference pixels, if necessary; and

adding correction data to the reference pixels.

47. The method of claim 46, further comprising performing texturing operations for the macroblock.

48. An article of manufacture comprising:

an electronically accessible medium providing instructions that, when executed by one or more processors, cause the one or more processors to

receive a motion compensation command having associated correction data related to a macroblock;

storing the correction data in a memory block by block in row major order;

perform frame prediction operations in response to the motion compensation command;

read the correction data from the memory sub-block by sub-block in row major order; and

combine the correction data with results from the frame prediction operations to generate an output video frame.

49. The article of manufacture of claim 48, wherein the electronically accessible medium further comprises instructions that, when executed by one or more processors, cause the one or more processors to

generate a bounding box containing the macroblock; and

iterate the bounding box;

fetch reference pixels;

filter the reference pixels;

average the filtered reference pixels, if necessary; and

add correction data to the reference pixels.

50. The article of manufacture of claim 49, wherein the electronically accessible medium further comprises instructions that, when executed by one or more processors, cause the one or more processors to perform texturing operations for the macroblock.